SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION				ATTY. DOCKET NO. 57454-963		SERIAL NO. Divisional of Serial No. 09/903,735		
WW 1 3 2003 Hiroshi MAEDA, ET AL.								
(PTO-1449)				FILING DATE August 5, 20			GROUP To be assigned	
U.S. PATENT DOCUMENTS								
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME		CLASS	SUBCLASS	FILING DATE	
π	6,424,011	07/2002	Assaderaghi et al		257	350		
TI	6,255,151	07/2001	Fukuda et al		257	296		
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		FOR	EIGN PATE	NT DOCUMEN	VTS			
EXAMINER'S INITIALS	PATENT NO. DATE		COUNTRY		CLASS	SUBCLASS	Translation Yes No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
π	M. Igarashi, A. Harada, H. Amishiro, H. Kawashima, N. Morimoto, Y. Kusumi, T. Saito, A. Ohsaki, T. Mori, T. Fukada, Y. Toyoda, K. Higashitani, and H. Arima, "The Best Combination Of Aluminum and Copper Interconnects For a High Performance 0.18µm CMOS Logic Device," IEDM98, 1998, PP. 829-832.							
П	J. Heidenreich, D. Edelstein, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, T. McDevitt, A. Stamper, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, S. Luce, and J. Slattery, "Copper Dual <u>Damascene</u> Wiring for Sub-0.25µm CMOS Technology," PP. 13-15.							
EXAMINER DATE CONSIDERED 09/03/04								

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.